SDR MK1.5 changes list

ok	Both Ethernet chips on-board: ENC28J60 and KSZ8851SNL	
ok	INT signal to Ethernet module (besides SPI bus)	
ok	Speaker connector (to spell IP address numbers). Use UC3B0512 chip audio codec output pins and filter topology from datasheet (although it is just merely a GPIO for UC3B0256 chip)	
ok	CDCE913 Clock synthesizer on board for DRC	
ok	PoE compatible magnetic RJ45 Jack. PoE pins and external SDR power supply input signals to a “PoE regulator board” header pins	
ok	Route USB signals as 90 ohm diff. pair + GND plane underneath	
X	DGND and AGND separated with 100nH inductor?	Currently 0-ohm resistor tie
ok	Check, what signals are needed by Elonics E4000 for extension board	PA0..2 (GPIO), TWI, Power, PB2..5 (UART), PA3..4 (codec), power
ok	Extension board headers after lowpass filter section making possible to replace entire lowpass filter section	
ok	Spare clock signals from synthesizer to extension connector	
X	Y1 freq testpoint for clock synth (for crystal calibration)	Can be measured through Y2 clock output on extension connector
ok	Filter/extension bord management signals. Have to allow configuration of a extension board (will have driving cpu, ATiny or such). - TWI - Also all relevant power buses! - GPIO - UART	
ok	Go through AVR Schematic Checklist document for AT32UC3B0256	
ok	USB power and data signals through common-mode filter	
ok	Route AOUT to SSC interface RX_DATA function 0 pin (PB07), but also route BOUT to RX_DATA function 4 (PA11) through 0 ohm resistor.	Used for double-speed SPI for chB when 0512 chip used
ok	600Ohm Ferrite bead decoupling before DRC and DVGA analog VCC in-s	
ok	Rework master power to 3.3V	
ok	PIN-diode limiter / ESD Protection diode for inputs	
ok	Double-check USB noise filtering measures. Check 10MHz region.	
ok	Power switching for one DVGA to prevent excessive USB current drawing (ENC28J60 takes about 250mA full steam) (Micrel Ethernet chip takes around 80mA)	Jumper on board
ok	External DRC sync signal, so multiple boards could be daisy-chained phase-correct way	
X	RF shield on board?	Does not fit and not needed
ok	Check against Elonics hardware design guide	
ok	Check all voltages and signal levels for all the chips (there should no more be anything over 3.3, but few need 1.8V)	
ok	TWI signals through common mode ferrite	
X	Ferrite beads for DVGA control signals?	Not needed
ok	SCC, SPI and TWI bushes shall have 20 ohm resistors between signals to prevent noise	Currently 0 ohm on most signals, as traces are short
X	Rotary encoder for program LO changes? (HID device?!)	To the extension board
X	Check, what signal caused excessive noise on spectrum when touched.	New CPU
ok	JTAG bus to header	
ok	Take care, that bootloader could be executed without opening the box	(UC3B HWBE signal cant be tied with resistor, as it will then enter loader on powerup as well)
ok	4-Layer board with separate ground and power plances	
ok	SPI bus and spare chipselect (NPCS2) to extension header	
ok	SSC interface to the separate header (both, AOUT and BOUT signals) for possible second CPU connection	
ok	Double-check decoupling capacitors for all power traces	
ok	Double-check reset signals on all chips	
ok	Reset+HWBE+Button1 on board (have to be on the edge somewhere)	
X	Programmable attenuator for signals	Not fitted, dynamic range is now 24 bit
ok	Check the SCK signal short (naming problem) on DRC and Atmel	Gone away by CPU change
ok	Prerforated prototype area for PoE circuitry DIY	
ok	AVCC bypasses for DVGA chips through ferrite beads near chip	
ok	FTDI FT232 cable pinout for UART signals on extension connector	
ok	TWI and SPI pull-ups	
ok	PA11 to GPIO signals on extension	